**Report HW 0 ECE-111**

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# **2-to-4 decoder**

1. **Behavioral level**
   1. **SystemVerilog Code**

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* 1. **RTL SchematicA diagram of a decodeo

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  2. **Post mapping schematicA computer screen shot of a diagram

     AI-generated content may be incorrect.**
  3. **Resource Usage**

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**Number of ALUT:** 4 (6 I/O pins)

4 ALUTs each for the output, which there are 4 outputs

**Number of Functions:** 4 (2 input function)

Require 4 2-input function for each output (2 input for sel\_0 sel\_1)

* 1. **Modelsim simulation results**

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**A screenshot of a computer program

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The decoder transform the 2 bit input into 1 in the corresponding position.

1. **Dataflow level**
   1. **SystemVerilog Code**

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* 1. **RTL schematic**

**A diagram of a computer program

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* 1. **Post mapping schematic**

**A computer screen shot of a diagram

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* 1. **Resource usage**

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* 1. **Modelsim simulation result (same as behavioral level simulation result)**

1. **Gatelevel**
   1. **SystemVerilog Code**

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* 1. **RTL schematic**

**A diagram of a circuit

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* 1. **Post mapping schematic**

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* 1. **Resource usage**

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* 1. **Modelsim simulation result (same as behavioral level simulation result)**

# **2-to-1 Mux**

1. **Behavioral level**
   1. **RTL schematic**

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* 1. **Post mapping schematic**

**A diagram of a computer

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* 1. **Resource usage**

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**Number of ALUT:** 1 (4 I/O pins)

2:1 MUX design need only one ALUT for the single output

**Number of Functions:** 1 (3 input function)

Require 1 3-input function for the single output, with 3 input in\_0, in\_1, and sel

* 1. **Modelsim simulation result**

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**A screenshot of a computer program

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The 2-to-1 mux choose one of the two value based on the select value 0 or 1.

1. **Dataflow level**
   1. **RTL schematic**

**A diagram of a circuit

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* 1. **Post mapping schematic**

**A diagram of a computer

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* 1. **Resource usage**

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* 1. **Modelsim simulation result (same as behavioral level simulation result)**

1. **Gatelevel**
   1. **RTL schematic**

**A diagram of a circuit

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* 1. **Post mapping schematic**

**A diagram of a computer

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* 1. **Resource usage**

**A screenshot of a computer

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* 1. **Modelsim simulation result (same as behavioral level simulation result)**

# **Full Adder**

1. **Behavioral level**
   1. **RTL schematic**

**A diagram of a circuit

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* 1. **Post mapping schematic**

**A diagram of a computer

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* 1. **Resource usage**

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**Number of ALUT:** 2 (5 I/O pins)

Full adder design need two ALUT for adding with 3 input and 2 output pins.

**Number of Functions:** 2 (3 input function)

Each output depends on all three inputs, thus 2 functions with 3 inputs

* 1. **Modelsim simulation result**

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The full adder takes in two value with a carryin bit and return the sum for the current digit with a carryout bit if needed.

1. **Dataflow level**
   1. **RTL schematic**

**A diagram of a circuit

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* 1. **Post mapping schematic**

**A diagram of a computer

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* 1. **Resource usage**

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* 1. **Modelsim simulation result (same as behavioral level simulation result)**

1. **Gatelevel**
   1. **RTL schematic**

**A diagram of a circuit

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* 1. **Post mapping schematic**

**A diagram of a computer

AI-generated content may be incorrect.**

* 1. **Resource usage**

**A screenshot of a computer

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* 1. **Modelsim simulation result (same as behavioral level simulation result)**